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EXAMINER	
ROMANO, JOHN J	

ART UNIT	PAPER NUMBER
2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,971	HINES ET AL.	
	Examiner	Art Unit	
	John J Romano	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *see office action*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-8** are pending in this action.

Information Disclosure Statement

1. The Information Disclosure Statements filed on April 30th, 2002, August 26th, 2002, September 16th, 2004, October 12th, 2004, October 18th, 2004, October 22nd, 2005 and January 10th, 2005 has been considered.

Drawings

2. The drawings are objected to because the specification, Page 5, Paragraph [0078] refers to Figure 10 wherein, the"...subgraph replacement table 1000..." is referenced, but the label "1000" is omitted on the drawing. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must

be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim **6** is objected to because of the following informalities: Claim 6 recites the limitation "...in which, in which...", wherein the second occurrence should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims **1, 2, 5** and **8** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by chou et al., "Control Generation for Embedded Systems Based on Composition of Modal Processes" (Art of record and hereinafter **Chou**).

6. In regard to claim **1**, **Chou** discloses:

- "*A method of implementing a software application on a target hardware architecture having a first and second processing resource and a predetermined interaction protocol between the first and second processing resources, comprising: designing a software system independent of the target hardware architecture* ..." (E.g., see Figure 9(b) & Page 46, "Abstract"), wherein control information (predetermined interaction protocol) is synthesized or implemented on a multi-processor architecture having a first and second processing resource, wherein the software system is independent of the target hardware architecture.
- "...*the software system including a first and a second functional object each performing a predetermined action*..." (E.g., see Figure 1(b) & Page 48, Section 2.2 "abstract control types"), wherein two functional components (objects) each performing a predetermined action are illustrated.
- "...*a coordination object for regulating control and dataflow interactions between the first and second functional objects*..." (E.g., see Figure & Page 48, Section 2.2 "abstract control types"), wherein a design tool that uses high-level primitives called Abstract Control Types (ACT) accomplishes control and dataflow interactions between the first and second functional objects.

- "...*a control object for handling control interactions between one of the functional objects and the coordination object*, and *a dataflow object for handling dataflow interactions between one of the functional objects and the coordination object...*" (E.g., see Figure 5 & Page 49, Section 3.1 "graph formulation"), wherein a control object for handling control interactions between one of the functional objects and the coordination object, and a dataflow object for handling dataflow interactions between one of the function objects and the coordination object are illustrated.
- "...*creating a software graph based on the software system, in which the first functional object is represented as a first set of software nodes in which a first action and a first mode within the first functional object are represented as a first action node and a first mode node, respectively, and in which the second functional object is represented as a second set of software nodes, in which a second action and a second mode within the second functional object are represented as a second action node and a second mode node, respectively...*" (E.g., see Figure 6 & Page 49, Section 3.2 "ACT expansion"), wherein a ACTs are applied across the processes which include a software graph (Figure 6) based on the software system in

which a first and second object (bumper, wheels, etc.) are represented by action and mode nodes.

- "*...the coordination object is represented as a set of coordination nodes in which a coordination action is represented as a coordination action node and a coordination mode is represented as a coordination mode node...*" (E.g., see Figure 5 & Page 49, Section 3.1 "graph formulation"), wherein a system of modes and primitive constraints can be represented by a bipartite graph implementing coordination comprising a mode node and an action node.
- "*...the dataflow object is represented as a dataflow edge connecting one of the software nodes within the first and second sets of software nodes to one of the coordination nodes within the set of coordination nodes, and the control object is represented as a control edge connecting one of software nodes within the first and second sets of software nodes to one of the coordination nodes within the set of coordination nodes...*" (E.g., see Figure 5 & Page 49, Section 3.1 "graph formulation"), wherein a control object for handling control interactions between one of the functional objects and the coordination object, and a dataflow object for handling dataflow interactions between one of the function objects and the

coordination object are illustrated via the edges connecting the software nodes with the coordination nodes.

- "*...creating a hardware graph based on the target hardware architecture wherein the first processing resource is represented as a first hardware node, the second processing resource is represented as a second hardware node and the interaction protocol is represented as a hardware edge connecting the first and second hardware nodes...*" (E.g., see Figure 8(d) & Page 52, Section 5.3 "Examples"), wherein a multi-processor architecture is graphed comprising a first and second processing resource being represented by a first and second hardware node and the interaction protocol is represented as a hardware edge.
- "*...mapping the software graph to the hardware graph, wherein the first set of software nodes is mapped to the first hardware node, the second set of software nodes is mapped to the second hardware node, the set of coordination nodes are mapped to the first hardware node and one of the control and dataflow edges is mapped to the hardware edge.*" (E.g., see Figure 8 & Page 52, Section 5.3 "Examples"), wherein the software graph is mapped to the hardware graph, comprising the first set on the first hardware node and the second set of software nodes mapped to the second hardware node (8b) and

the set of coordination nodes accordingly, wherein the dataflow and control edges are shown via the hardware edge ACT and the shadow nodes (8c).

7. In regard to claim **2**, the rejections of base claim **1** are incorporated. Furthermore, **Chou** discloses:

- "*...replacing the one of the control and dataflow edges that has been mapped to the hardware edge with a first replacement node mapped to the first hardware node and a second replacement node mapped to the second hardware node, for implementing said edge in terms of the interaction protocol provided by the target hardware architecture.*" (E.g., see Figure 8 c) & Page 52, Section 5.2, "control communication"), wherein the first and second shadow modes are added for all external constraint sources (interaction protocol provided by the target hardware architecture).

8. In regard to claim **5**, the rejections of base claim **1** are incorporated. Furthermore, **Chou** discloses:

- "*...implementing the software system on a second target hardware architecture having three processing resources and a predetermined first interaction protocol between a first and a second processing resource of the three processing resources and a predetermined second interaction protocols between the second and a third of the three processing resources further*

comprising: creating a second hardware graph based on the second target hardware architecture wherein the first of the three processing resource is represented as a first hardware node, the second processing resource of the three processing resources is represented as a second hardware node, the third processing resource of the three processing resources is represented as a third hardware node, ..." (E.g., see Figure 8(a-d) & Page 51, "Distributed mode manager"), wherein three hardware sources are illustrated, wherein three hardware nodes represent three processing resources and the ACTs represent a first and second interaction protocol between the processors.

- "*...the predetermined first interaction protocol is represented as a first hardware edge connecting the first and second hardware nodes, and the predetermined second interaction protocol is represented as a second hardware edge connecting the second and third hardware nodes; mapping the software graph to the second hardware graph, wherein the first set of software nodes are mapped to the first hardware node, the second set of software nodes are mapped to the third hardware node, the set of coordination nodes are mapped to the second hardware node...*" (E.g., see Figure 8(a-d) & Page 51, "control communication"), wherein the predetermined first and second interaction protocols are represented as first and second

hardware edges, wherein the ACTs ((a,b,c,λ)) comprise the primitives which dictate the interaction protocol.

- "...*a crossing dataflow edge connecting one of the coordination nodes to one of the software nodes of the first set of software nodes is mapped to the first hardware edge, and a crossing control edge connecting one of the coordination nodes to one of the software nodes of the second set of software nodes is mapped to the second hardware edge...*" (E.g., see Figure 8(c) & Page 52, Section 5.3 "Examples"), wherein a dataflow and control flow edge is mapped to the shadow modes.
- "...*replacing the crossing dataflow edge with a first data replacement node mapped to the first hardware node and a second data replacement node mapped to the second hardware node for implementing the crossing dataflow edge in terms of the predetermined first interaction protocol; and replacing the crossing control edge with a first control replacement node mapped to the second hardware node, and a second control replacement node mapped to the third hardware node for implementing the crossing control edge in terms of the predetermined second interaction protocol...*" (E.g., see Figure 8(c) & Page 52, Section 5.3 "Examples"), wherein a dataflow and control flow edge is mapped to the shadow modes which are added for all the external constraint sources.

9. In regard to claim **8**, **Chou** discloses:

- "*A system for generating an executable version of a software application for use with a target hardware architecture having a plurality of processing resources and an interaction protocol for controlling information exchanges between the processing resources, the software application being designed independent of the target hardware architecture, the system comprising: a software application design tool for building software applications based on functional requirements and explicit coordination characteristics...*" (E.g., see Figure 9(b) & Page 46, "Abstract"), wherein control information (predetermined interaction protocol) is synthesized or implemented on a multi-processor architecture having a first and second processing resource, wherein the software system is independent of the target hardware architecture, wherein executable code built in software design tool is inherent to the process.
- "*...a software graphing tool that generates a coordination graph based on the software application, in which first and second functional components of the software application are represented as first and second software nodes, respectively, first and second software nodes having a node type that is based on a function performed by the respective functional component, and in which an information exchange between the*

first and second functional components is represented as a software edge connecting the first and second software nodes, and the software edge has an edge type that is based on the type of information exchange it represents..." (E.g., see Figure 5 & Page 49, Section 3.1 "graph formulation"), wherein a control object for handling control interactions between one of the functional objects and the coordination object, and a dataflow object for handling dataflow interactions between one of the function objects and the coordination object are illustrated via the edges, comprising the types of edges based on the information it represents, connecting the software nodes with the coordination nodes, wherein the nodes represent actions and modes.

- "*...a hardware graphing tool for generating a target hardware graph based on the target hardware architecture, in which first and second computational resources are represented as first and second hardware nodes, respectively, and the interaction protocol which controls information exchanges between the processing resources is represented as a hardware edge connecting the first and second software nodes...*" (E.g., see Figure 8(d) & Page 52, Section 5.3 "Examples"), wherein a multi-processor architecture is graphed comprising a first and second processing resource being represented by a first and

second hardware node and the interaction protocol is represented as a hardware edge.

- "...*a mapping tool in which the first and second software nodes are mapped to first and second hardware nodes, respectively, and the software edge is mapped to the hardware edge, and first and second replacement nodes are mapped to first and second hardware nodes, each replacement node representing a functional replacement component that will implement the information exchange represented by the software edge in terms of the interaction protocol represented by the hardware edge, and will pass any interactions to the respective first and second components*..." (E.g., see Figure 8 & Page 52, Section 5.3 "Examples"), wherein the software graph is mapped to the hardware graph, comprising the first set on the first hardware node and the second set of software nodes mapped to the second hardware node (8b) and the set of coordination nodes accordingly, wherein the software edges are shown according to their interaction protocol.
- "...*a code synthesizing tool in which an executable version of the first functional and functional replacement components will be generated for use on the first processing resource and an executable version of the second functional and functional replacement components will be generated for use on the*

second processing resource." (E.g., see Figure 6 & Page 49, Section 3.2 "ACT expansion"), wherein a ACTs are applied across the processes which include a software graph (Figure 6) based on the software system in which a first and second object (bumper, wheels, etc.) are represented by action and mode nodes.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims **3, 4, 6** and **7** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chou**.

12. In regard to claim **3**, the rejections of base claim **2** are incorporated. But, **Chou** does not expressly disclose "*...the first and second replacement nodes are chosen from a set of replacement nodes based upon the type of edge being replaced and the interaction protocol provided by the target hardware architecture.*" But, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to abstractly clarify a set of different

protocols on the graph. The motivation to do so was provided by **Chou** (Section 5 "Distributed mode manager", page 51), where "...several synchrony options can be supported", however to avoid "over-specification" Chou focuses on one in particular. Therefore, it would have been obvious to one of ordinary skill in the art to include different nodes in a set according to the particular implementation used where over-specification was not a concern. Thus, it would have been **obvious** to one of ordinary skill in the art, at the time the invention was made to include "*...the first and second replacement nodes are chosen from a set of replacement nodes based upon the type of edge being replaced and the interaction protocol provided by the target hardware architecture*" in order to further clarify or specify the coordination of the system.

13. In regard to claim **4**, the rejections of base claim **3** are incorporated. Furthermore, **Chou** discloses:

- "*...the first processing resource based on the first set of software nodes, the set of coordination nodes, and the first replacement node that were mapped to the first hardware node, and generating implementation code for the second processing resource based on the second set of software nodes that were mapped to the second hardware node.*" (E.g., see Figure 8(a-d)), wherein the first and second set of software nodes, the set of coordination nodes, and replacement nodes were mapped to the first and second hardware node.

But **Chou** does not explicitly disclose "...*generating implementation code...*". However, it would have been obvious to generate implementation code, at the time the invention was made, to one of ordinary skill in the art, as **Chou** teaches a design tool for distributed embedded systems that uses high-level primitives called Abstract Control Types and an algorithm for synthesizing runtime code to implement control information coherence within and between distributed processors ("Abstract").

14. In regard to claim **6**, the rejections of base claim **5** are incorporated. But, **Chou** does not expressly disclose "...*in which the first and second data replacement nodes and the first and second control replacement nodes are chosen from a set of replacement nodes based upon the interaction protocols provided by the target hardware architecture.*" But, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to abstractly clarify a set of different protocols on the graph. The motivation to do so was provided by **Chou** (Section 5 "Distributed mode manager", page 51), where "...several synchrony options can be supported", however to avoid "over-specification" Chou focuses on one in particular. Therefore, it would have been obvious to one of ordinary skill in the art to include different nodes in a set according to the particular implementation used where over-specification was not a concern. Thus, it would have been **obvious** to one of ordinary skill in the art, at the time the invention was made to include "...*in which the first and second data replacement nodes and the first and second control replacement nodes are chosen from a set of replacement nodes based upon the interaction protocols*

provided by the target hardware architecture." in order to further clarify or specify the coordination of the system.

15. In regard to claim **7**, the rejections of base claim **6** are incorporated. Furthermore, **Chou** discloses:

- "*...the first processing resource based on the first set of software nodes and the first control replacement node; generating implementation code for the second processing resource based on the set of coordination nodes, the second data replacement node, and the first control replacement node; and generating implementation code for the third processing resource based on the second set of software nodes and the second control replacement node.*" (E.g., see Figure 8(a-d)), wherein the first and second set of software nodes, the set of coordination nodes, and replacement nodes were mapped to the first and second hardware node.

But **Chou** does not explicitly disclose "*...generating implementation code...*". However, it would have been obvious to generate implementation code, at the time the invention was made, to one of ordinary skill in the art, as **Chou** teaches a design tool for distributed embedded systems that uses high-level primitives called Abstract Control Types and an algorithm for synthesizing runtime code to implement control information coherence within and between distributed processors ("Abstract").

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Romano whose telephone number is (571) 272-3872. The examiner can normally be reached on 8-5:30, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJR

TUAN DAM
SUPERVISORY PATENT EXAMINER